9. An electronic apparatus according to Claim 7, wherein said electronic apparatus comprises a camera.

10. An electronic apparatus according to Claim 7, further comprising a control circuit that controls said electronic apparatus, and wherein said control circuit includes a central processing unit.

REMARKS

Claims 1 through 10 are now presented for examination. Claims 1, 5, 7 and 10 have been amended to define still more clearly what Applicant regards as his invention, in terms which distinguish over the art of record. Claims 1 and 7 are the only independent claims.

Claims 5 and 10 have been rejected under 35 U.S.C. § 112, second paragraph, as indefinite in that the term "said control circuit" lacks antecedent basis. As amended, each of Claims 5 and 10 recites that the electronic apparatus comprises a control circuit and that the control circuit includes a central processing unit. It is therefore believed that Claims 5 and 10 as amended fully meet the requirements of 35 U.S.C. § 112, second paragraph.

Claims 1 and 4 have been rejected under 35 U.S.C. § 102(b), as anticipated by U.S. Patent No. 5,854,950 (Handa et al.). Claim 2 has been rejected under 35 U.S.C. § 103(a), as unpatentable over the Handa et al. in view of U.S. Patent No. 6,285,625

(Vogley). Claims 3 and 5 have been rejected under 35 U.S.C. § 103(a), as unpatentable over the Handa et al. in view of U.S. Patent No. 4,825,233 (Kanai et al.). Claim 6 has been rejected under 35 U.S.C. § 103(a), as unpatentable over the Handa et al. in view of Japanese Laid-Open Patent No. 06-250278 (Kitani).

Independent Claim 1 as amended is directed to electronic apparatus in which a clock circuit generates a clock signal having clock signal pulses generated at a predetermined cycle. A non-volatile memory circuit counts the clock signal pulses generated by the clock circuit and stores a count of the clock signal pulses.

In Applicant's view, Handa et al. discloses a data recording device capable of preventing the recording of incorrect date and time data on photographic film due to malfunction of the time counter that generates date and time data for recording. A drive of the data recording device has time counter that generates date and time data for recording. The count value of the date and time data generated by this time counter is stored in a storage circuit. Immediately prior to the operation that changes the count value of the time counter, the date and time data in the storage circuit and the counter value of the date and time data from the time counter are compared in a comparison judgment circuit. If the two do not agree, a malfunction detection signal which indicates that the time counter has malfunctioned is output to the driver and the recording of date and time data by liquid crystal display panel is stopped.

It is a feature of Claim 1 as amended that a non-volatile memory circuit both counts clock circuit generated clock pulses and stores a count of the clock pulses. Handa et

al. may teach that generated clock signals are counted and that the count value is stored. The Handa et al. arrangement, however, requires that the clock pulses be counted in a time counter 161 and that the count value of the time counter be stored in a storage circuit 33 separate from the time counter. As clearly disclosed at lines 52 through 62 of Handa et al., "Data recording device 30 is also equipped with comparison judgment circuit 34 which compares output 161(A) of time counter 161 and output 161(B) of the stored contents of storage circuit 33. If output 161(A) and output 161(B) are detected to not be the same by comparison judgment circuit 34, malfunction detection signal 34S is output from comparison judgment circuit 34 and is supplied to driver 162. When driver 162 receives signal 34S, drive of liquid crystal display panel 12 is stopped after that. As a result, recording performed by imprinting date and time data on photographic film 4 is not performed." Accordingly, storage circuit 33 could not provide a count value for comparison with the count value of the separate time counter 161 as required by Handa et al. if the storage circuit both counted clock pulses and stored a count of the clock pulses as in Claim 1. It is therefore believed that Claim 1 as amended is completely distinguished from Handa et al. and is allowable.

Claims 7 and 9 have been rejected under 35 U.S.C. § 103(a), as unpatentable over the Handa 'et al. in view of U.S. Patent No. 6,285,625 (Vogley). Claims 8 and 10 have been rejected under 35 U.S.C. § 103(a), as unpatentable over the Handa et al. in view of U.S. Patent No. 4,825,233 (Kanai et al.).

Independent Claim 7 as amended is directed to electronic apparatus in which a time-keeping circuit keeps time and a ferroelectric memory circuit forms and stores a time signal concerning time kept by the time-keeping circuit.

In Applicant's opinion, Vogley discloses a synchronous dynamic random access memory that operates in synchronism with differential clock signals (CLK and /CLK). A timing and control circuit compares the complementary differential clock signals (CLK and /CLK) to generate an internal clock signal (CLKI) so as to compensate for degradations in the differential clock signals (CLK and /CLK). Utilizing the internal timing signal (CLKI) avoids employing more complex circuits that must operate in synchronism with the edges of both differential clock signals (CLK and /CLK).

According to the invention of Claim 7 as amended, a ferroelectric memory circuit forms and stores a time signal concerning time kept by a time-keeping circuit. As discussed with respect to Claim 1, Handa et al. only teaches a time counter that generates date and time data for recording and a separate storage circuit that stores the count value of the date and time data for comparison with the time counter data to detect malfunctions of the time counter. It is not seen that Handa et al. which requires forming of date and time data that is performed separately from the storage of the data and time data for malfunction detection in any manner teaches or suggests that a ferroelectric memory both forms and stores a time signal as in Claim 7.

Vogley discloses a clocking arrangement for a random access memory in which complementary differential clock signals are compared to generate a single internal

timing signal for clocking the memory and teaches that both a ferroelectric memory and an EEPROM may both benefit from this clock timing arrangement. The Vogley disclosure, however, is limited to teaching that a ferroelectric memory may benefit from a memory clocking arrangement in which first and second complementary differential clock signals provide an internal memory timing signal but is devoid of any suggestion of a ferroelectric memory forming and storing a time signal for time-keeping.

Neither Handa et al. nor Vogley suggest anything about a ferroelectric memory that both forms and stores a timing signal of time kept by a time-keeping circuit as in Claim 7. It is not seen that the addition of Vogley's memory clocking using complementary differential clock signals provide an internal memory timing signal to Handa et al.'s generating date and time data in a time counter that is separate from a storage circuit for the date and time data could possibly suggest the feature of a ferroelectric memory that both forms and stores a time signal for time keeping of Claim 7. It is therefore believed that Claim 7 as amended is completely distinguished from any combination of Handa et al. and Vogley and is allowable.

A review of the other art of record has failed to reveal anything which, in Applicant's opinion, would remedy the deficiencies of the art discussed above, as references against the independent claims herein. Those claims are therefore believed patentable over the art of record.

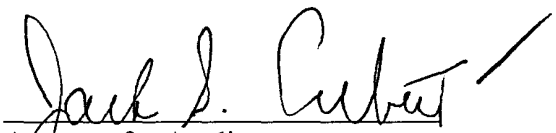
The other claims in this application are each dependent from one or another of the independent claims discussed above and are therefore believed patentable for the

same reasons. Since each dependent claim is also deemed to define an additional aspect of the invention, however, the individual reconsideration of the patentability of each on its own merits is respectfully requested.

In view of the foregoing amendments and remarks, Applicant respectfully requests favorable reconsideration and early passage to issue of the present application.

Applicants' attorney, C. Phillip Wrist, may be reached in our Washington, D.C. office by telephone at (202) 530-1010. All correspondence should continue to be directed to our below listed address.

Respectfully submitted,



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VERSION WITH MARKINGS TO SHOW CHANGES MADE TO THE CLAIMS

1. (Amended) An electronic apparatus comprising:

a clock circuit that generates a clock signal having clock signal pulses generated at a predetermined cycle; and

a non-volatile memory circuit [that counts] for counting clock signal pulses generated by said clock circuit and [stores the counted] storing a count of the clock signal pulses.

5. An electronic apparatus according to Claim 4, further comprising a control circuit that controls said electronic apparatus, and wherein said control circuit includes a central processing unit.

7. (Amended) An electronic apparatus comprising:

a time-keeping circuit that keeps time: and

a ferroelectric memory circuit that forms and stores a time signal concerning time kept by said time-keeping circuit.

10. An electronic apparatus according to Claim 7, further comprising a control circuit that controls said electronic apparatus, and wherein said control circuit [comprises] includes a central processing unit.